Gregory L. Moss

Lab Solutions Manual

for

Lab Manual: A Design Approach

to accompany

DIGITAL SYSTEMS:

PRINCIPLES AND APPLICATIONS

Eleventh Edition

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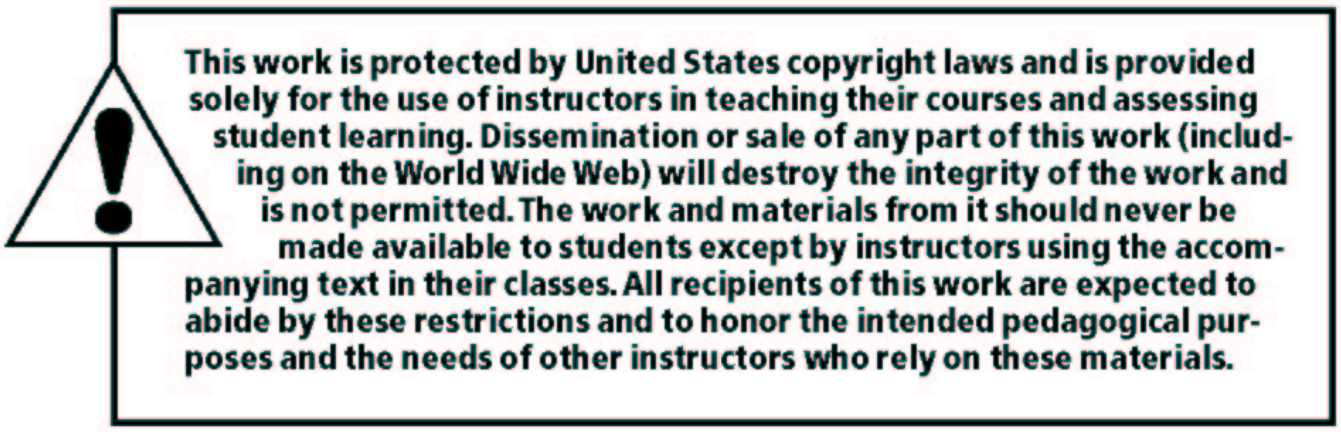

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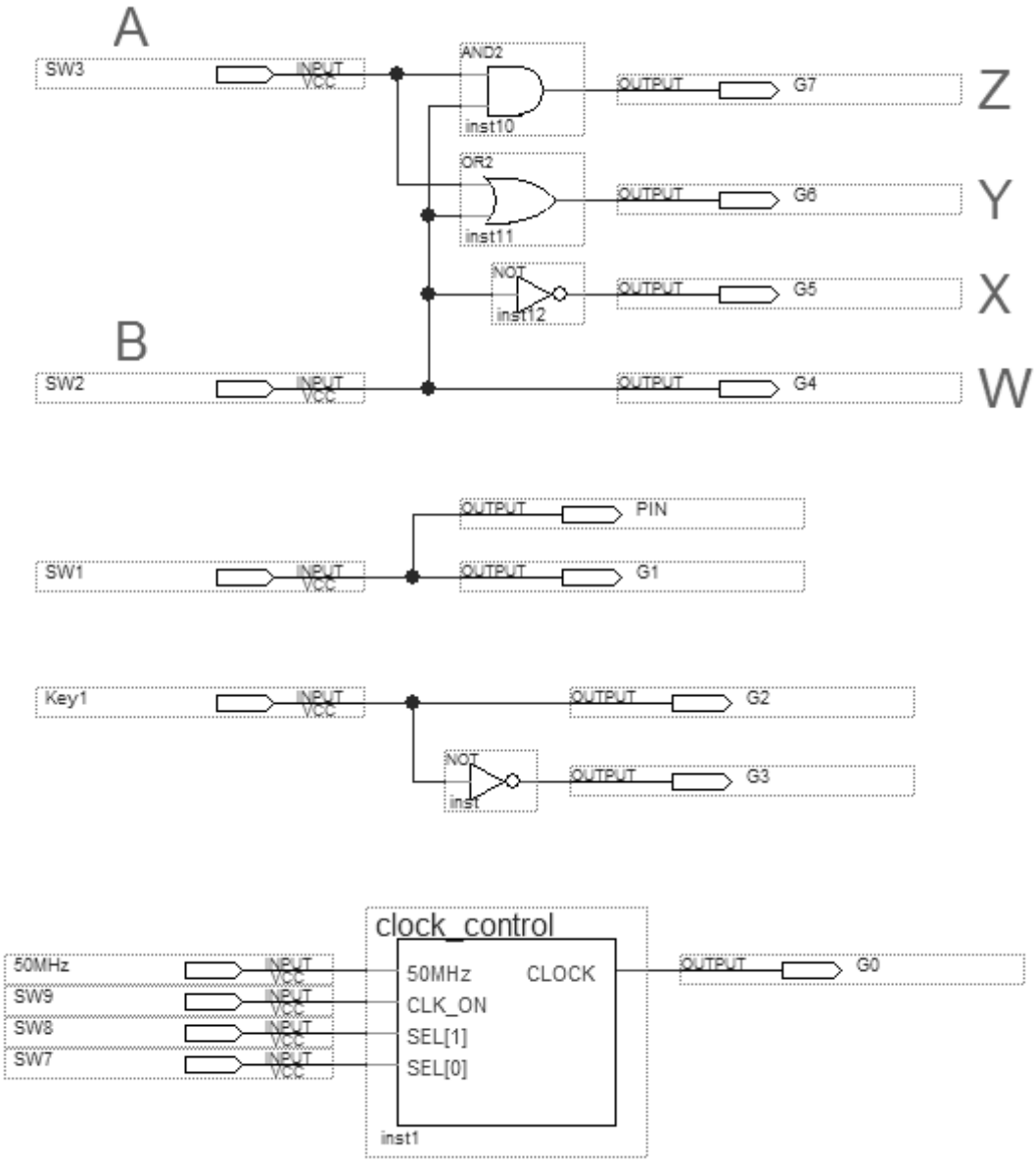
CONTENTS

Unit 1 Introduction to the DE0, DE1, or DE2 Development & Education Board

Project: Intro2DE0, Intro2DE1, or Intro2DE2



1.3 Logic Switches

Board	DE0	DE1	DE2
# switches	10	10	18

Logic Switch SW1	LEDG1 (on/off)	Logic level (high/low)	Voltage at connector pin
Down	Off	Low	~0 V
Up	On	High	~3.3 V

1.4 LEDs

LED label	Color	DE0	DE1	DE2
LEDR	Red	0	10	18
LEDG	Green	10	8	9

1.5 Pushbuttons → Normally High

Board	DE0	DE1	DE2
Pushbutton	3	4	4

Pushbutton #1	LEDG2 (on/off)	LEDG3 (on/off)
Normal	On	Off
Pressed	Off	On

1.6 Clock

CLK_ON (SW9)	1	1	1	1	0
SEL[1..0] (SW8, SW7)	00	01	10	11	XX
$freq_{G0}$	0.5 Hz	5 Hz	25 Hz	50 Hz	0 Hz

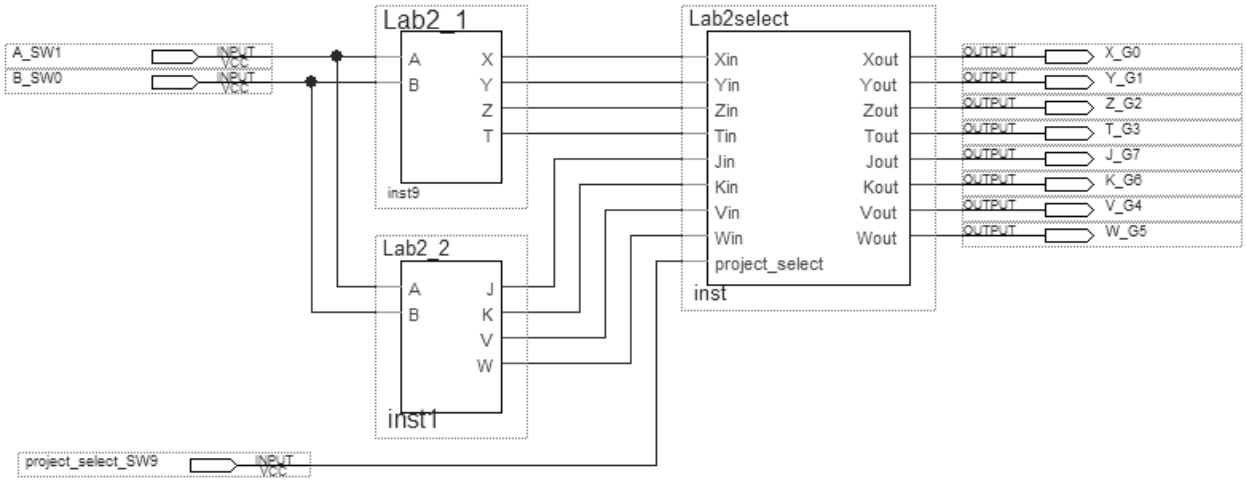
1.7 Simple logic circuits

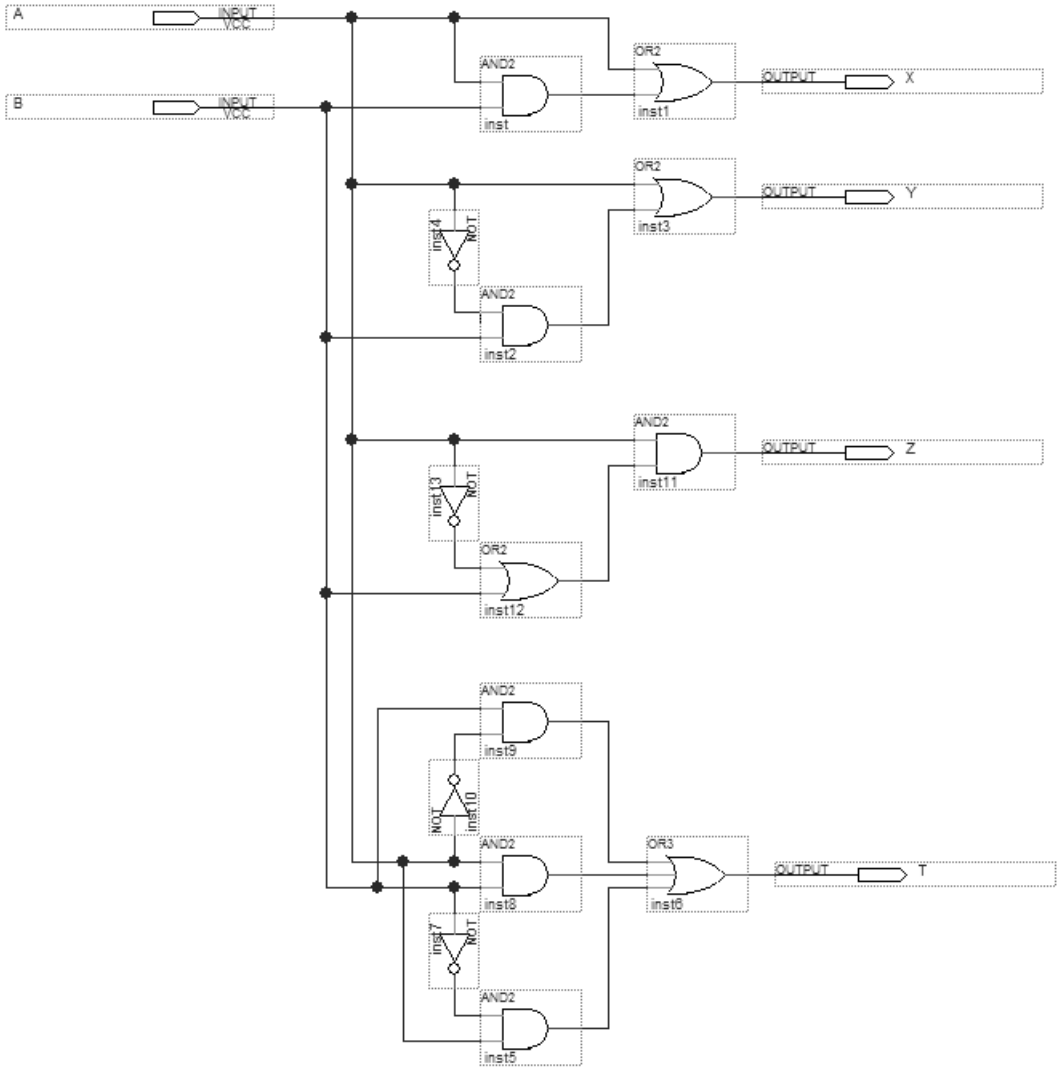
A (SW3)	B (SW2)	W (LEDG4)	X (LEDG5)	Y (LEDG6)	Z (LEDG7)
0	0	0	1	0	0
0	1	1	0	1	0
1	0	0	1	1	0
1	1	1	0	1	1

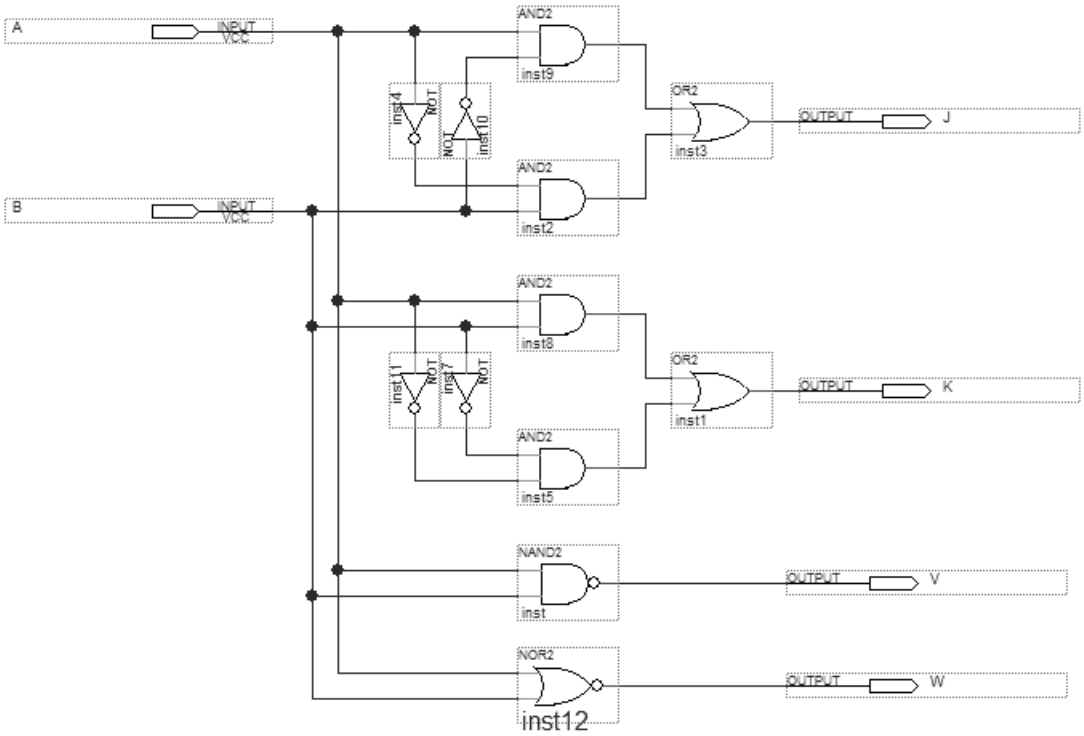
$W = B$ $X = \overline{B}$ $Y = A + B$ $Z = A\ B$

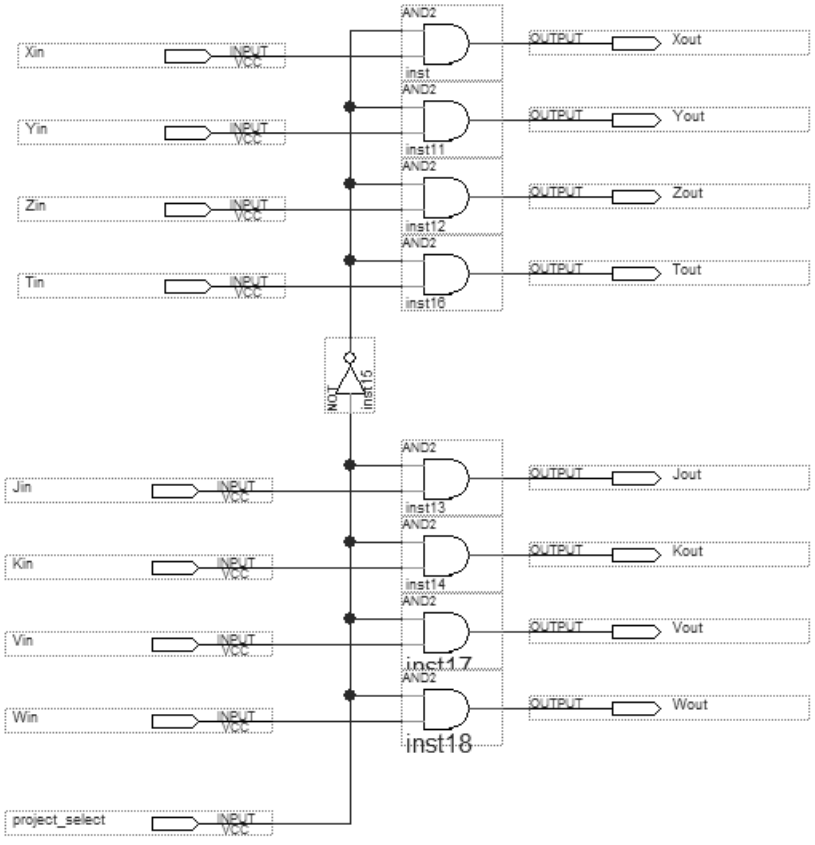
Unit 2 Testing Combinational Logic Circuits Using DE0, DE1, or DE2 Boards

Project: Lab2DE0, Lab2DE1, or Lab2DE2






A
INPUT
VCC
B
INPUT
VCC
AND2
inst9
AND2
inst2
NOT
inst4
NOT
inst10
OR2
inst3
OUTPUT
J
AND2
inst8
AND2
inst5
NOT
inst11
NOT
inst7
OR2
inst1
OUTPUT
K
NAND2
inst
OUTPUT
V
NOR2
inst12
OUTPUT
W


Xin
INPUT
VCC
Yin
INPUT
VCC
Zin
INPUT
VCC
Tin
INPUT
VCC
AND2
inst
AND2
inst11
AND2
inst12
AND2
inst16
OUTPUT
Xout
OUTPUT
Yout
OUTPUT
Zout
OUTPUT
Tout
NOT
inst15
Jin
INPUT
VCC
Kin
INPUT
VCC
Vin
INPUT
VCC
Win
INPUT
VCC
project_select
INPUT
VCC
AND2
inst13
AND2
inst14
AND2
inst17
AND2
inst18
OUTPUT
Jout
OUTPUT
Kout
OUTPUT
Vout
OUTPUT
Wout

2.1 Simple circuits

$X = A + A\,B = A$ $\qquad$ $Y = A + \overline{A}\,B = A + B$

$Z = A\,(\overline{A} + B) = A\,B$ $\qquad$ $T = \overline{A}\,B + A\,B + A\,\overline{B} = A + B$

A	B	T	Z	Y	X	J	K	W	V
0	0	0	0	0	0	0	1	1	1
0	1	1	0	1	0	1	0	0	1
1	0	1	0	1	1	1	0	0	1
1	1	1	1	1	1	0	1	0	0

2.2 More circuit functions

$V = \overline{\overline{A}\,\overline{B}}$ $\qquad$ $W = \overline{\overline{A} + B}$

$J = A\,\overline{B} + \overline{A}\,B = A \oplus B$ $\qquad$ $K = A\,B + \overline{A}\,\overline{B} = \overline{A \oplus B}$

Unit 3 Schematic Capture & Analysis of Combinational Logic Circuits

3.1 Example 3-1 (see Lab Manual Example 3-1 & Quartus Tutorial 1 – Schematic)

3.2 Equivalent circuits

(a) V = W? true

V = A (B + C)

W = A C + A B

(b) X = Y? true

$X = \overline{A}\ \overline{B} + A\ B + A\ C$

$Y = \overline{A}\ \overline{B} + A\ B + \overline{B}\ C$

A	B	C	V	W	X	Y
0	0	0	0	0	1	1
0	0	1	0	0	1	1
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	0	0	0
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

3.3 DeMorgan's theorem

(a) p1 = p2 = p3? true

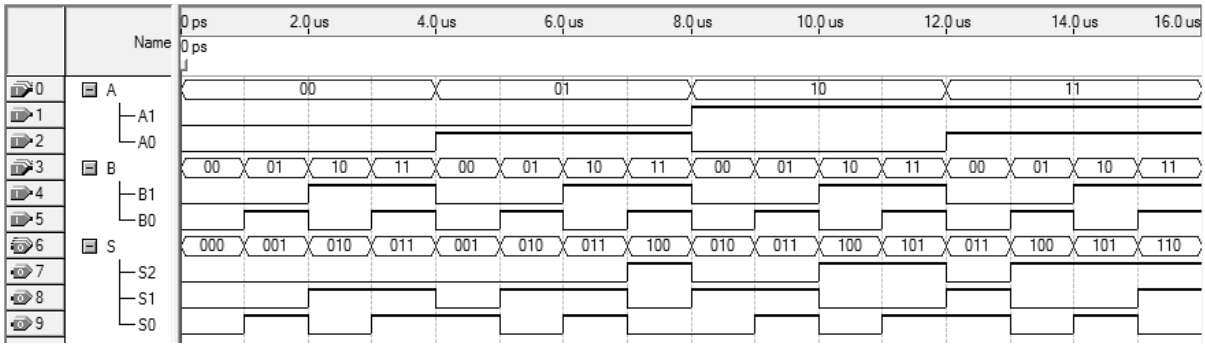
$p1 = \overline{a}\ \overline{b}$ $p2 = \overline{a}\ \overline{b}$ $p3 = \overline{a + b}$

(b) q1 = q2 = q3? true

$q1 = \overline{a} + \overline{b}$ $q2 = \overline{a} + \overline{b}$ $q3 = \overline{a\ b}$

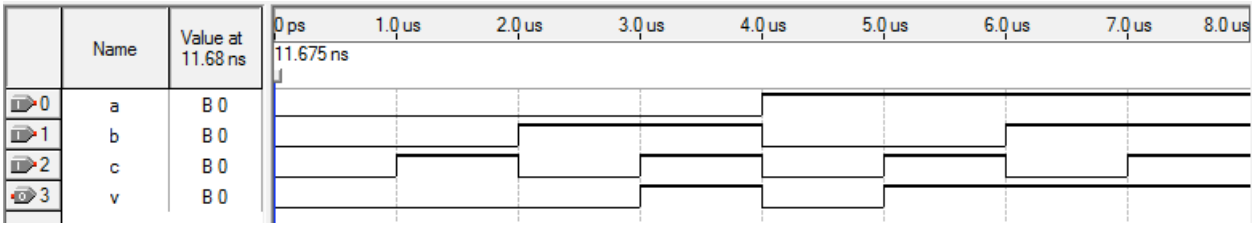
a	b	p	q
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	0

3.4 2-bit adder



Unit 4 Design and Simulation of Combinational Circuits

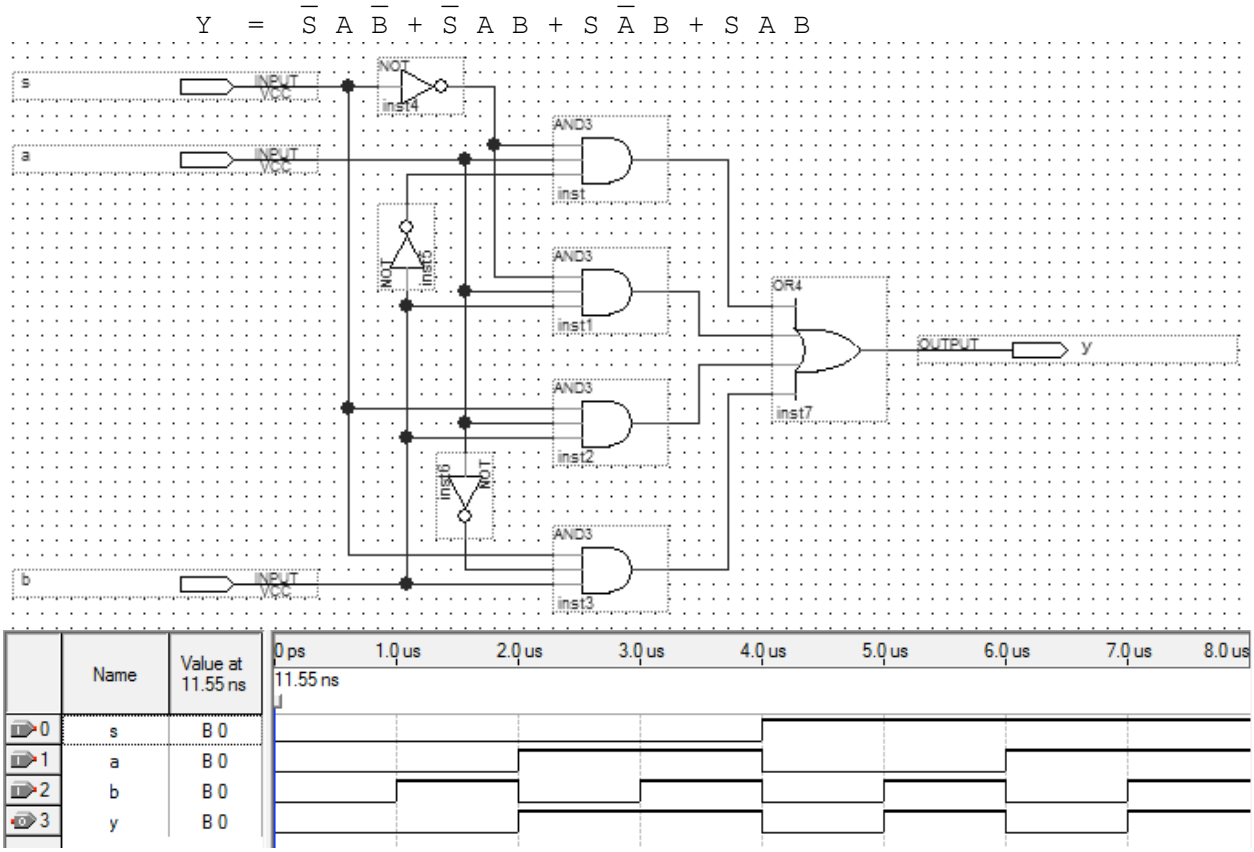
4.1 Majority vote (see Lab Manual Example 4-1 & Quartus Tutorial 2 – Simulation)



4.2 Two-input multiplexer

S	A	B	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

$$Y = \overline{S}\,A\,\overline{B} + \overline{S}\,A\,B + S\,\overline{A}\,B + S\,A\,B$$

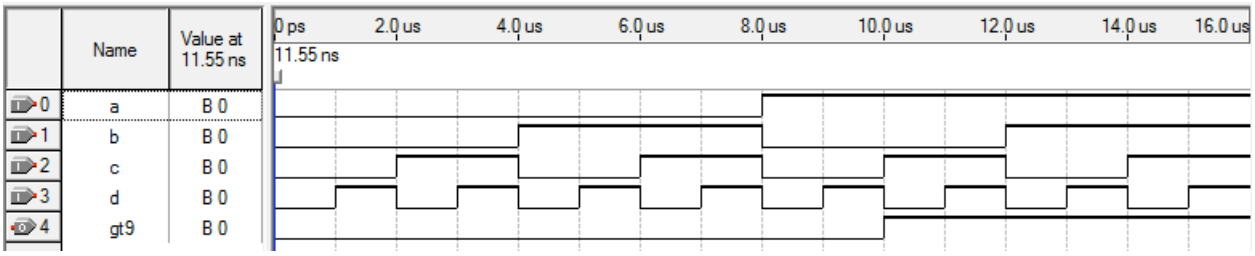


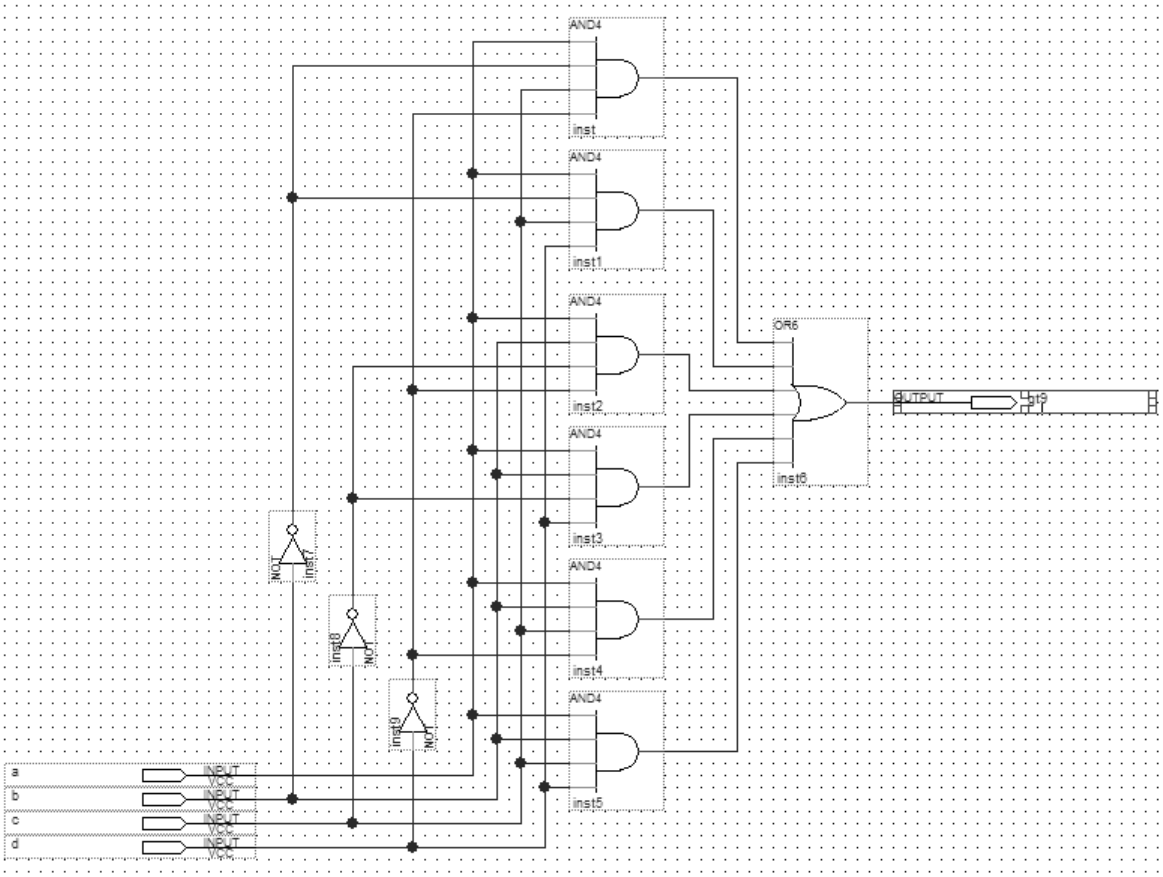
4.3 Non-BCD input

A	B	C	D	GT9
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$$GT9 = A\,\overline{B}\,C\,\overline{D} + A\,\overline{B}\,C\,D + A\,B\,\overline{C}\,\overline{D} + A\,B\,\overline{C}\,D$$

$$+ A\,B\,C\,\overline{D} + A\,B\,C\,D$$

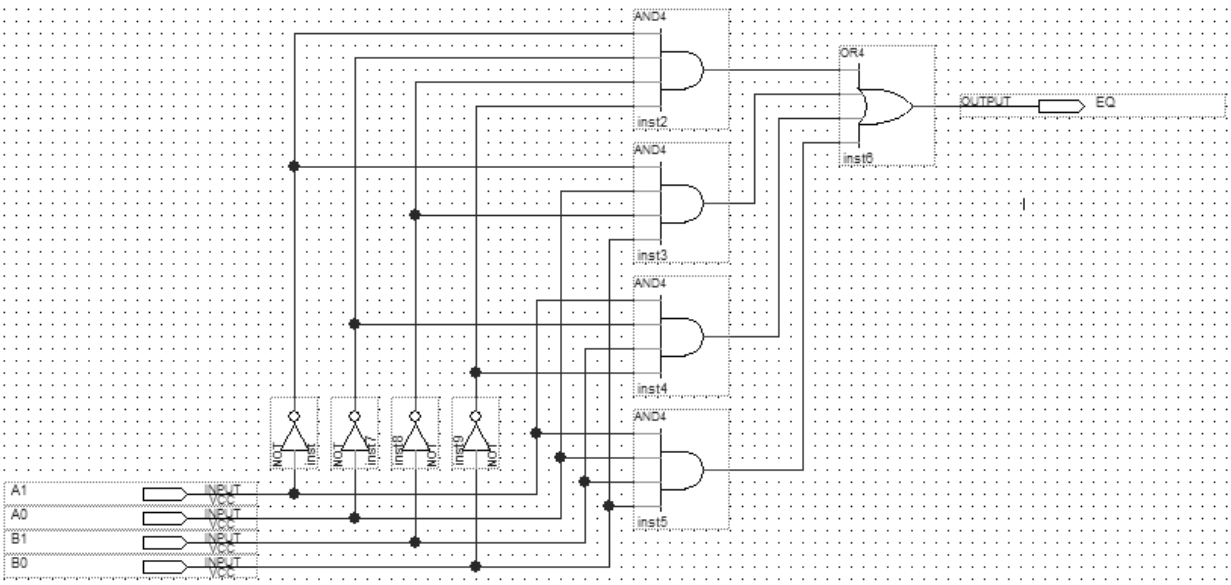




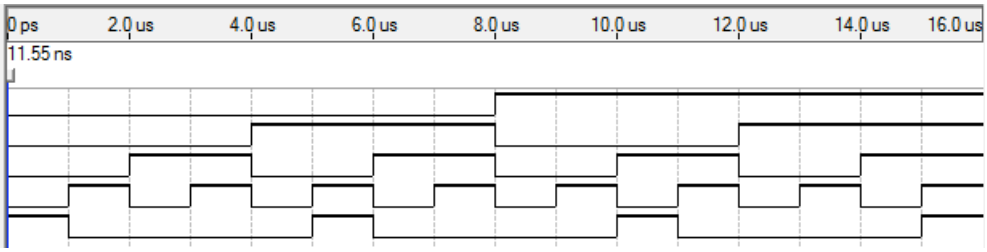
4.4 Two-bit comparator

A1	A0	B1	B0	EQ
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

$$EQ = \overline{A1}\ \overline{A0}\ \overline{B1}\ \overline{B0} + \overline{A1}\ A0\ \overline{B1}\ B0 + A1\ \overline{A0}\ B1\ \overline{B0} + A1\ A0\ B1\ B0$$



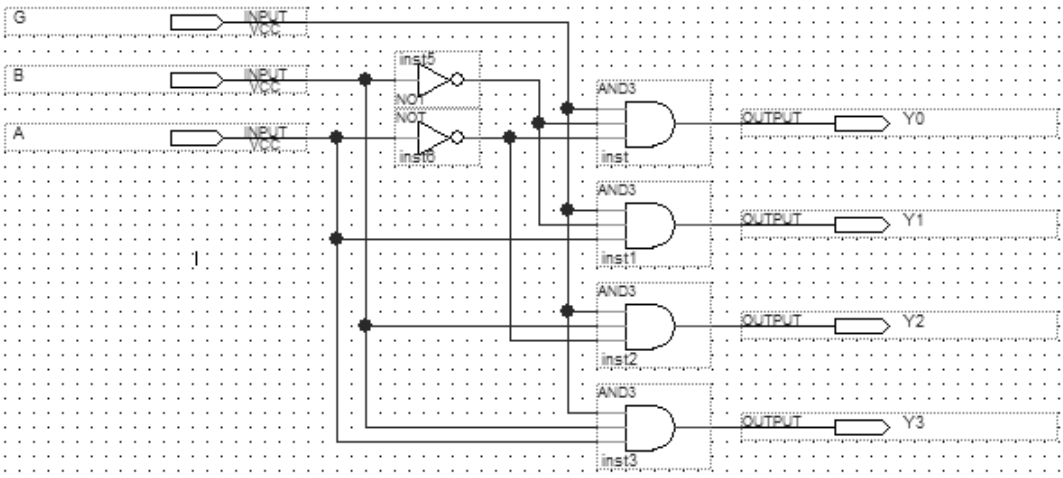
	Name	Value at 11.55 ns
0	A1	B 0
1	A0	B 0
2	B1	B 0
3	B0	B 0
4	EQ	B 1

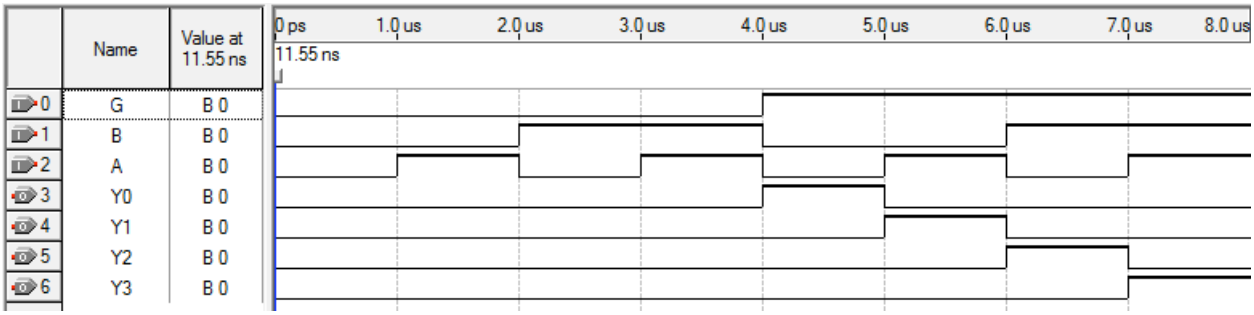


4.5 Binary number detector

$Y0 = G\,\overline{B}\,\overline{A}$ $\quad$ $Y1 = G\,\overline{B}\,A$

$Y2 = G\,B\,\overline{A}$ $\quad$ $Y3 = G\,B\,A$



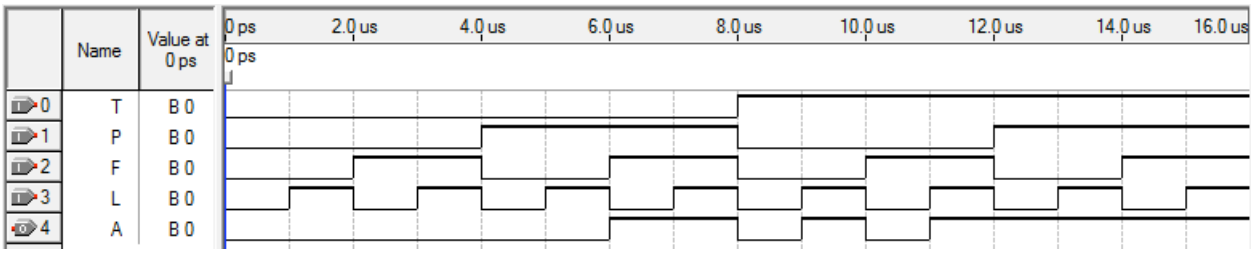


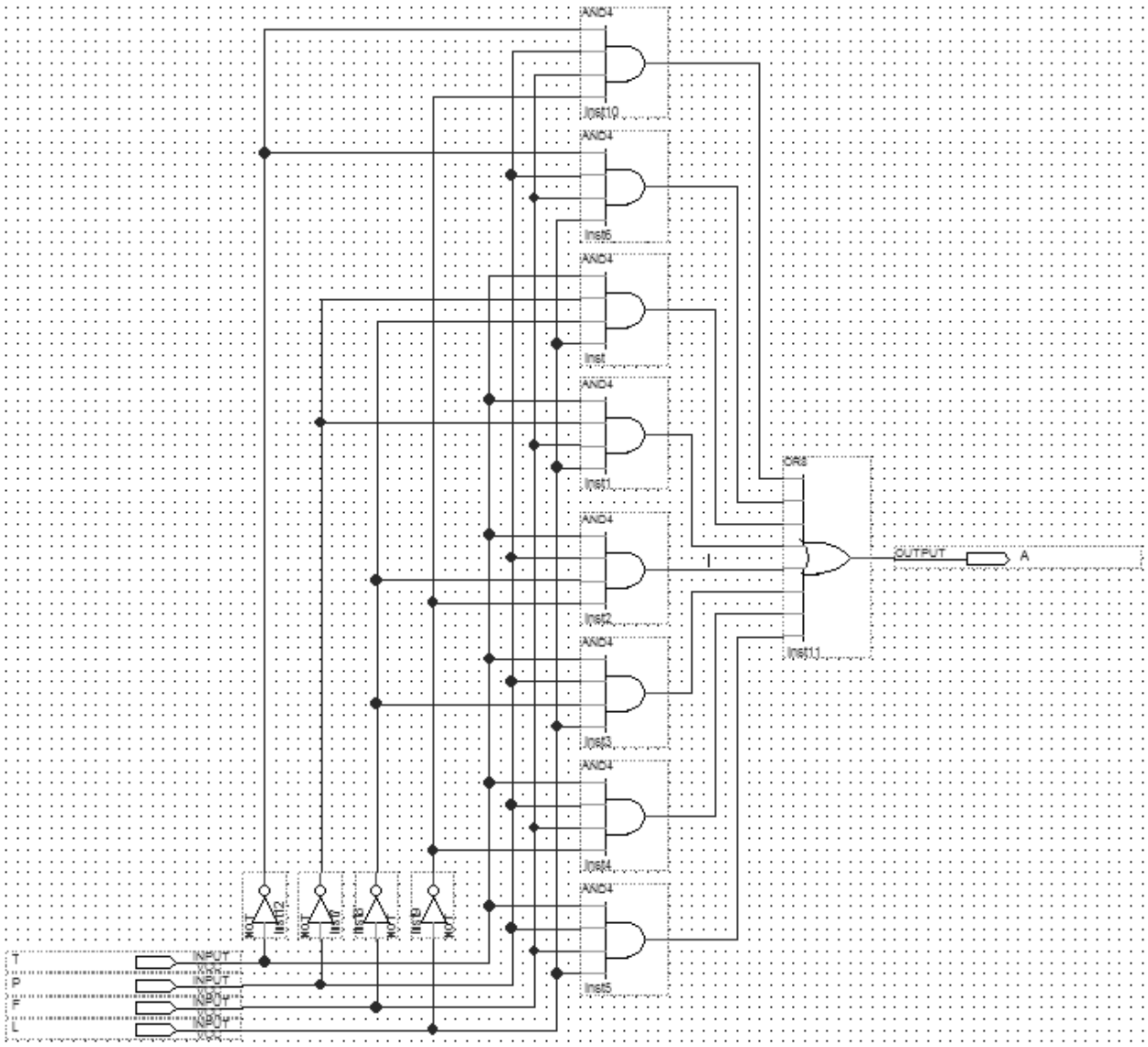
4.6 Alarm circuit

T	P	F	L	A
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$$A = \overline{T}\,P\,F\,\overline{L} + \overline{T}\,P\,F\,L + T\,\overline{P}\,\overline{F}\,L + T\,\overline{P}\,F\,L$$

$$+ \; T\,P\,\overline{F}\,\overline{L} + T\,P\,\overline{F}\,L + T\,P\,F\,\overline{L} + T\,P\,F\,L$$

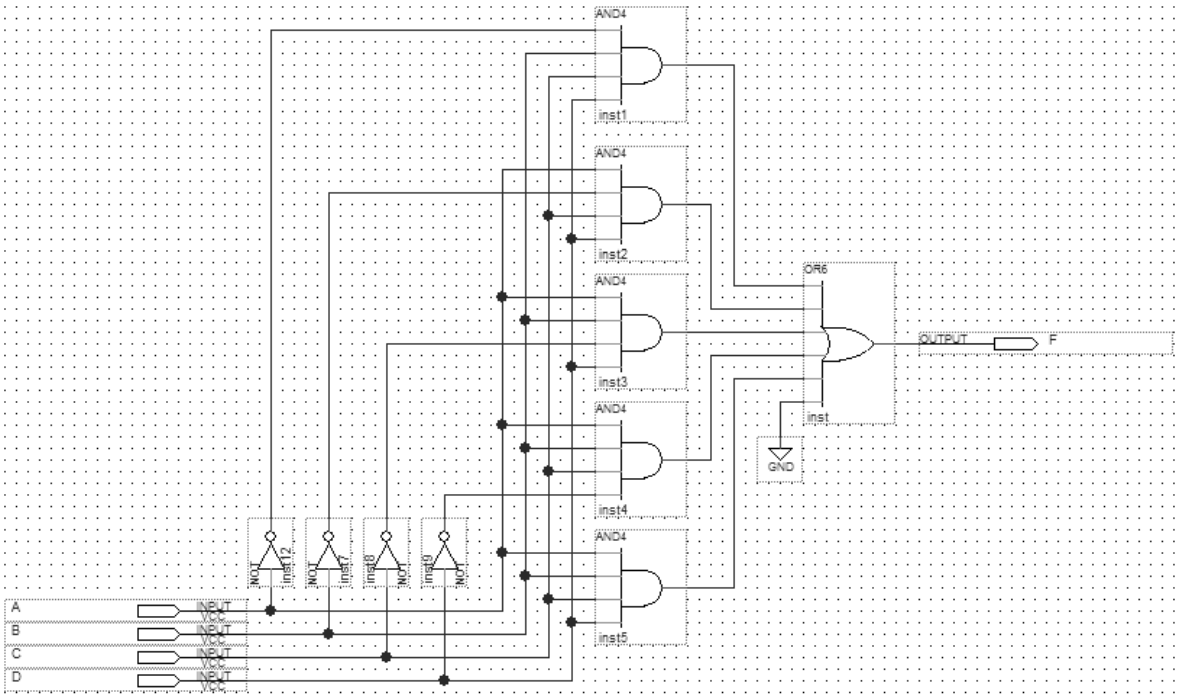


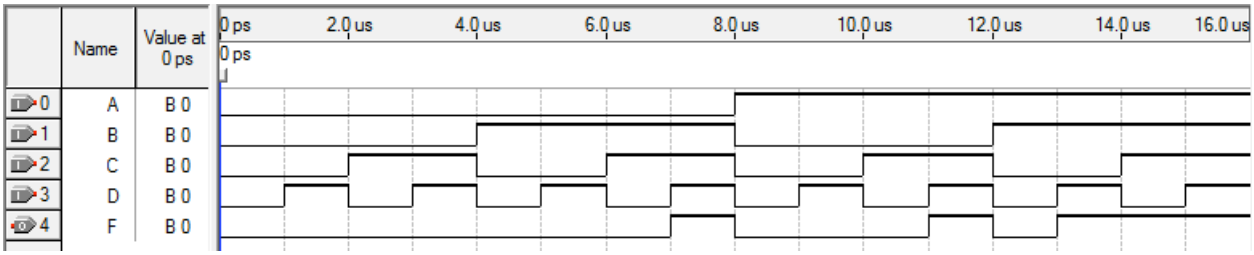

AND4
I06\10
AND4
Inst6
AND4
Inst
AND4
I\61
AND4
Inst2
AND4
I06\3
AND4
I06\4
AND4
I\65
OR6
Inst11
OUTPUT
A
INPUT
INPUT
INPUT
INPUT
T
P
F
L

4.7 Elevator control

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$$F = \overline{A}\,B\,C\,D + A\,\overline{B}\,C\,D + A\,B\,\overline{C}\,D + A\,B\,C\,\overline{D} + A\,B\,C\,D$$

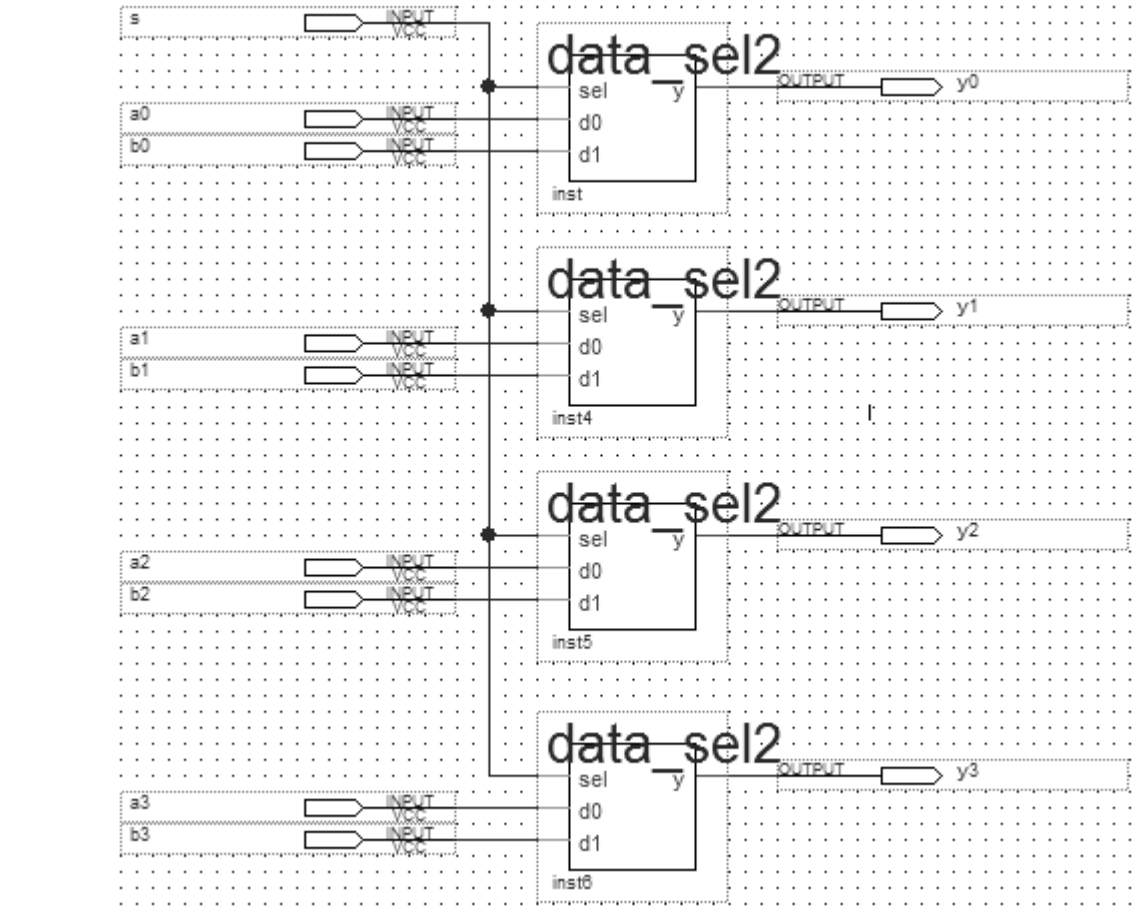


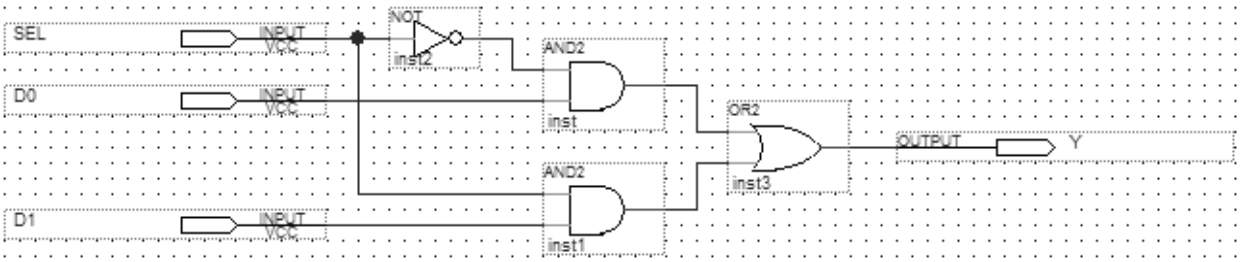


Unit 5 Creating Hierarchical Logic Circuits

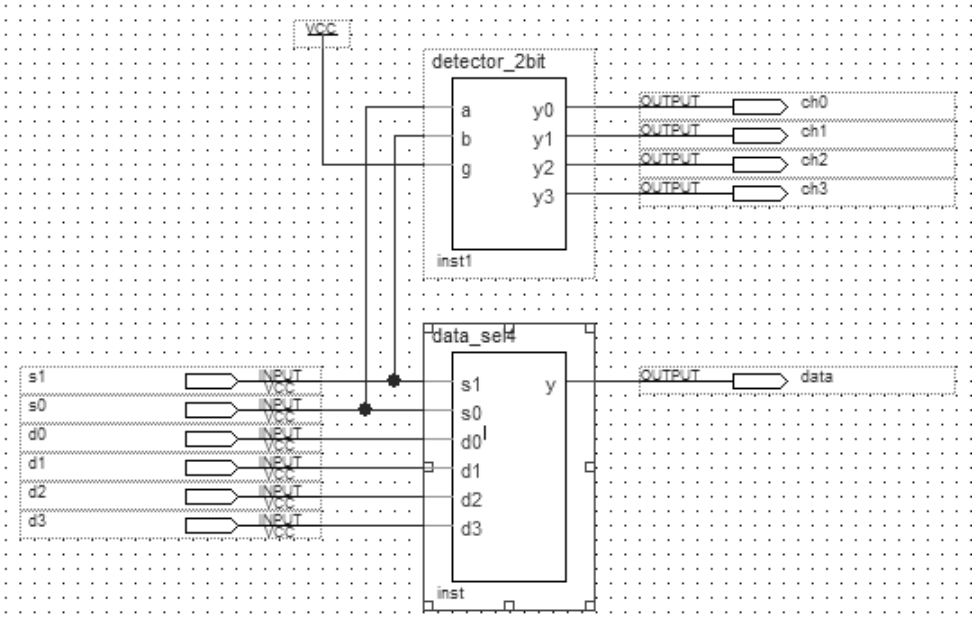
5.1 1-out-of-4 data selector (see Lab Manual Example 5-1 & Quartus Tutorial 3 – Hierarchical)

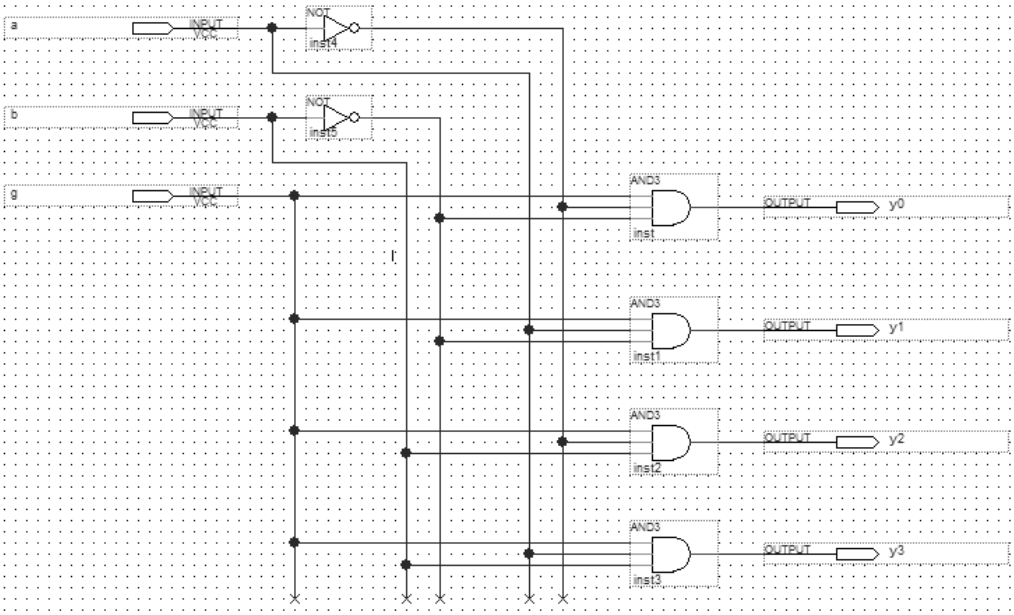
5.2 2-channel, 4-bit multiplexer

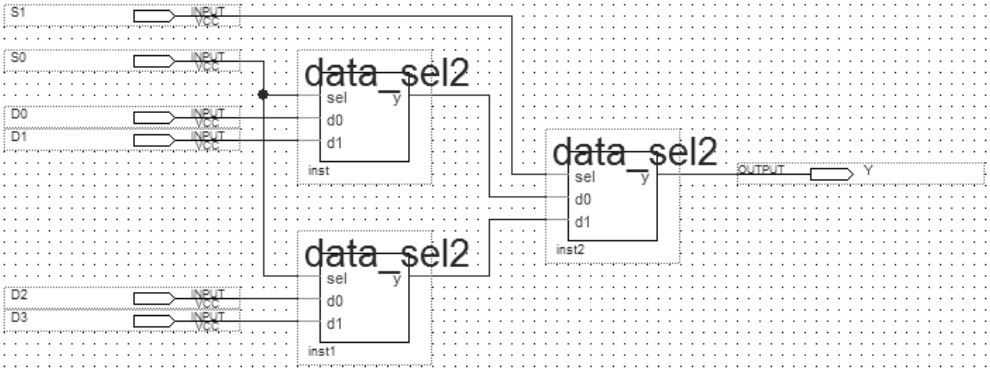




5.3 Multiplexer & decoder







5.4 3-bit decoder