library ieee;

use ieee.std\_logic\_1164.all;

entity and2\_gate is

port (A, B: in Std\_Logic; C: out Std\_Logic);

end and2\_gate;

architecture Boolean\_Equation of and2\_gate is

begin

C <= A and B;

end Boolean\_Equation;

library ieee;

use ieee.std\_logic\_1164.all;

entity or2\_gate is

port (A, B: in Std\_Logic; C: out Std\_Logic);

end or2\_gate;

architecture Boolean\_Equation of or2\_gate is

begin

C <= A or B;

end Boolean\_Equation;

library ieee;

use ieee.std\_logic\_1164.all;

entity xor2\_gate is

port (A, B: in Std\_Logic; C: out Std\_Logic);

end xor2\_gate;

architecture Boolean\_Equation of xor2\_gate is

begin

C <= A xor B;

end Boolean\_Equation;

library ieee;

use ieee.std\_logic\_1164.all;

entity Add\_half\_vhdl is

port (a, b: in std\_logic; c\_out, sum: out std\_logic);

end Add\_half\_vhdl;

architecture Structure of Add\_half\_vhdl is

component and2\_gate

port (A, B: in Std\_Logic; C: out Std\_Logic);

end component;

component xor2\_gate

port (A, B: in Std\_Logic; C: out Std\_Logic);

end component;

begin

G1: xor2\_gate port map (a, b, sum);

G2: and2\_gate port map (a, b, c\_out);

end Structure;

library ieee;

use ieee.std\_logic\_1164.all;

**entity** Add\_full\_vhdl **is**

**port** (a, b, c\_in: **in** std\_logic; c\_out, sum: **out** std\_logic);

**end** Add\_full\_vhdl;

arc**h**itecture Structure **of** Add\_full\_vhdl **is**

**signal** w1, w2, w3: std\_logic;

**component** or2\_gate

**port** (a, b: in std\_logic; c: **out** std\_logic);

**end** **component**;

comp**o**nent Add\_half\_vhdl

**port** (a, b: **in** std\_logic; c\_out, sum: **out** std\_logic);

**end** **component**;

**begin**

M0: Add\_half\_vhdl **port map** (w2, c\_in, w3, sum);

M1: Add\_half\_vhdl **port map** (a, b, w1, w2);

G1: or2\_gate **port map** (w1, w3, c\_out);

**end** Structure;

**library** ieee;

**use** ieee.std\_logic\_1164.all;

**entity** Add\_rca\_4\_vhdl **is**

**port** (A, B: **in** Std\_Logic\_vector (3 **downto** 0); c\_in: **in** Std\_Logic;

c\_out: **out** Std\_Logic; sum: **out** Std\_Logic\_vector (3 **downto** 0));

**end** Add\_rca\_4\_vhdl;

**architecture** Structure **of** Add\_rca\_4\_vhdl **is**

**signal** c\_in1, c\_in2, c\_in3: Std\_Logic;

**component** Add\_full\_vhdl

**port** (a, b, c\_in: **in** Std\_Logic; c\_out, sum: **out** Std\_Logic);

**end component**;

**begin**

M0: Add\_full\_vhdl **port map** (a(0), b(0), c\_in, c\_in1, sum(0));

M1: Add\_full\_vhdl **port map** (a(1), b(1), c\_in1, c\_in2, sum(1));

M2: Add\_full\_vhdl **port map** (a(2), b(2), c\_in2, c\_in3, sum(2));

M3: Add\_full\_vhdl **port map** (a(3), b(3), c\_in3, c\_out, sum(3));

**end** Structure;

**library** ieee;

**use** ieee.std\_logic\_1164.all;

**entity** Add\_rca\_8\_vhdl **is**

**port** (a, b: in Std\_Logic\_Vector (7 **downto** 0); c\_in: **in** Std\_Logic;

c\_out: **out** Std\_Logic; sum: **out** Std\_Logic\_Vector (7 **downto** 0));

**end** Add\_rca\_8\_vhdl;

**architecture** Structure **of** Add\_rca\_8\_vhdl **is**

**signal** c\_in4: Std\_Logic;

**component** Add\_rca\_4\_vhdl

**port** (a, b: **in** Std\_Logic\_Vector (3 **downto** 0); c\_in: **in** Std\_Logic;

c\_out: **out** Std\_Logic; sum: **out** Std\_Logic\_Vector (3 **downto** 0));

**end component**;

**begin**

M0: Add\_rca\_4\_vhdl **port map** (a(3 downto 0), b(3 **downto** 0), c\_in, c\_in4, sum(3 **downto** 0 ));

M1: Add\_rca\_4\_vhdl **port map** (a(7 downto 4), b(7 **downto** 4), c\_in4, c\_out, sum(7 **downto** 4 ));

**end** Structure;