

```
entity binary_adder is  
port (Sum: out Std_Logic_Vector (3 downto 0); C_out: Std_Logic);  
      A, B: in Std_Logic_Vector (3 downto 0); C_in: in Std_Logic);  
end binary_adder;
```

```
architecture Dataflow of binary_adder is  
begin  
      C_out & Sum <= A + B + ("000"&C_in);  
end Dataflow;
```