

```
// D flip-flop without reset
module D_FF (Q, D, Clk);
  output   Q;
  input    D, Clk;
  reg      Q;
  always @ (posedge Clk)
    Q <= D;
endmodule
```

```
// D flip-flop with active-low, asynchronous reset (V2001, V2005)
module DFF (output reg Q, input D, Clk, rst);
  always @ (posedge Clk, negedge rst)
    if (!rst) Q <= 1'b0;    // Same as: if (rst == 0)
    else Q <= D;
endmodule
```

---