**library** ieee;

**use** ieee.std\_logic\_1164.all;

**entity** decoder\_2x4\_gates\_vhdl **is**

**port** (A, B, enable: in std\_logic; D: **out** std\_logic\_vector (0 **to** 3));

**end** decoder\_2x4\_gates\_vhdl;

**architecture** Structure **of** decoder\_2x4\_gates\_vhdl **is**

signal A\_not, B\_not, enable\_not: Std\_Logic;

**component** inv\_gate

**port** (B: **out** std\_logic; A: **in** std\_logic);

**end** **component**;

**component** nand3\_gate

**port** (D: **out** std\_logic; A, B, C: **in** std\_logic);

**end** **component**;

**begin**

G1: inv\_gate **port map** (A\_not, A);

G2: inv\_gate **port map** (B\_not, B);

G3: inv\_gate **port map** (enable\_not, enable);

G4: nand3\_gate **port map** (D(0), A\_not, B\_not, enable\_not);

G5: nand3\_gate **port map** (D(1), A\_not, B, enable\_not);

G6: nand3\_gate **port map** (D(2), A, B\_not, enable\_not);

G7: nand3\_gate **port map** (D(3), A, B, enable\_not);

**end** Structure;

**library** ieee;

**use** ieee.std\_logic\_1164.all;

**entity** inv\_gate **is**

**port** (B: **out** std\_logic; A: **in** std\_logic);

**end** inv\_gate;

**architecture** Boolean\_Equation **of** inv\_gate **is**

**begin**

B <= **not** A;

**end** Boolean\_Equation;

**library** ieee;

**use** ieee.std\_logic\_1164.all;

**entity** nand3\_gate **is**

**port** (D: **out** std\_logic; A, B, C: **in** std\_logic);

**end** nand3\_gate;

**architecture** Boolean\_Eq **of** nand3\_gate **is**

**begin**

D <= **not** (A **and** B **and** C);

**end** Boolean\_Eq;