-- VHDL behavioral description of four-channel multiplexer

**entity** mux\_4x1\_beh\_vhdl is\_

**port** (m\_out: **out** Std\_Logic; in\_0, in\_1, in\_2, in\_3: **in** Std\_Logic;

**sel**: **in** Std\_Logic\_Vector (1 **downto** 0));

**end** mux\_4x1\_beh\_vhdl;

**Architecture** Behavioral **of** mux\_4x1\_beh\_vhdl is

**begin**

**process** (in\_0, in\_1, in\_2, in\_3, sel) **begin**

**case** sel **is**

**when** 0 => m\_out <= in\_0;

**when** 1 => m\_out <= in\_1;

**when** 2 => m\_out <= in\_2;

**when** 3 => m\_out <= in\_3;

**when** others => m\_out <= in\_0;

**endcase**;

**end** **process**;

**end** Behavioral;