**Library** IEEE;

**use** IEEE.Std\_Logic\_1164.all;

**entity** half\_adder\_vhdl **is**

**port** (S, C: **out** Std\_Logic; x, y: **in** Std\_Logic);

**end** half\_adder\_vhdl;

**architecture** Dataflow **of** half\_adder\_vhdl **is**

**begin**

S <= x **xor** y;

C <= x **and** y;

**end** Dataflow;

**Library** IEEE;

**use** IEEE.Std\_Logic\_1164.all;

**entity** full\_adder\_vhdl **is**

**port** (S, C: o**u**t Std\_Logic; x, y, z: **in** Std\_Logic);

**end** full\_adder\_vhdl;

**architecture** Structural **of** full\_adder\_vhdl **is**

**signal** S1, C1, C2: Std\_Logic;

**component** half\_adder\_vhdl **port** (S, C: **out** Std\_Logic; x, y: **in** Std\_Logic); **end** **component**;

**begin**

HA1: half\_adder\_vhdl **port map** (S => S1, C => C1, x => x, y => y);

HA2: half\_adder\_vhdl **port map** (S => S, C => C2, x => S1, y => z);

C <= C2 or C1;

**end** Structural;

**Library** IEEE;

**use** IEEE.Std\_Logic\_1164.all;

**entity** ripple\_carry\_4\_bit\_adder\_vhdl **is**

**port** (Sum: **out** Std\_Logic\_Vector (3 **downto** 0); C4: **out** Std\_Logic; A, B: **in**

Std\_Logic\_Vector (3 **downto** 0); C0: **in** Std\_Logic);

**end** ripple\_carry\_4\_bit\_adder\_vhdl;

**architecture** Structural **of** ripple\_carry\_4\_bit\_adder\_vhdl **is**

**signal** C1, C2, C3: Std\_Logic;

**component** full\_adder\_vhdl port (S, C: out Std\_Logic; x, y, z: in Std\_Logic);

**end component**;

**begin**

FA0: full\_adder\_vhdl

**port map** (S => Sum(0), C => C1, x => A(0), y => B(0), z => C0);

FA1: full\_adder\_vhdl

**port map** (S => Sum(1), C => C2, x => A(1), y => B(1), z => C1);

FA2: full\_adder\_vhdl

**port map** (S => Sum(2), C => C3, x => A(2), y => B(2), z => C2);

FA3: full\_adder\_vhdl

**port map** (S => Sum(3), C => C4, x => A(3), y => B(3), z => C3);

**end** Structural;