

```
entity mux_2x1_df_vhdl is
port (m_out: out Std_Logic; A, B, sel: in Std_Logic);
end mux_2x1_df_vhdl;
```

```
architecture Dataflow of mux_2x1_df_vhdl is
begin
    m_out <= A when sel = '1' else B;
end Dataflow;
```