**Library** IEEE;

**use** IEEE.Std\_Logic\_1164.all;

**entity** half\_adder\_vhdl **is**

**port** (S, C: **out** Std\_Logic; x, y: **in** Std\_Logic);

**end** half\_adder\_vhdl;

**architecture** Dataflow **of** half\_adder\_vhdl **is**

**begin**

S <= x **xor** y;

C <= x **and** y;

**end** Dataflow;