

-- Dataflow description of four-bit adder

**entity** binary\_adder **is**

**port** (Sum: **out** Std\_Logic\_Vector (3 **downto** 0); C\_out: **out** Std\_Logic;

A, B: **in** Std\_Logic\_Vector (3 **downto** 0); C\_in: **in** Std\_Logic);

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**end** binary\_adder;

**architecture** Dataflow **of** binary\_adder **is**

**begin**

C\_out & Sum <= A + B + ('000' & C\_in); -- Compatible word sizes

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**end** Dataflow;

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