**module** Add\_half (**input** a, b, **output** c\_out, sum),

**xor** G1(sum, a, b); // Gate instance names are optional

**and** G2(c\_out, a, b);

**endmodule**

**module** Add\_full **(input** a, b, c\_in, **output** c\_out, sum); // See Fig. 4.8

**wire** w1, w2, w3; // w1 is c\_out; w2 is sum

Add\_half M1 (a, b, w1, w2);

Add\_half M0 (w2, c\_in, w3, sum);

**or** (c\_out, w1, w3);

**endmodule**

**module** Add\_rca\_4(**input** [3:0] a, b, **input** c\_in **output** c\_out, **output** [3:0] sum);

**wire** c\_in1, c\_in3, c\_in4; // Intermediate carries

Add\_full M0 (a[0], b[0], c\_in, c\_in1, sum[0]);

Add\_full M1 (a[1], b[1], c\_in1, c\_in2, sum[1]);

Add\_full M2 (a[2], b[2], c\_in2, c\_in3, sum[2]);

Add\_full M3 (a[3], b[3], c\_in3, c\_out, sum[3]);

**endmodule**

**module** Add\_rca\_8(**input** [7:0] a, b, **input** c\_in, **output** c\_out, **output** [7:0] sum,)

**wire** c\_in4;

Add\_rca\_4 M0 (a[3:0], b[3:0], c\_in, c\_in4, sum[3:0]);

Add\_rca\_4 M1 (a[7:4], b[7:4], c\_in4, c\_out, sum[7:4]);

**endmodule**