-- VHDL behavioral description of two-channel multiplexer

**Library** IEEE;

**use** IEEE.Std\_Logic\_1164.all;

**entity** mux\_2x1\_beh\_vhdl **is**

**port** (m\_out: **out** Std\_Logic; A, B: **in** Std\_Logic;

sel: **in** Std\_Logic); -- select is a reserved word

**end** mux\_2x1\_beh\_vhdl;

**Architecture** Behavioral **of** mux\_2x1\_beh\_vhdl **is**

**begin**

**process** (A, B, sel) **begin**

**if** sel = '1' **then** m\_out <= A; **else** m\_out <= B; **end if**;

**end** **process**;

**end** Behavioral;