

-- Test bench with stimulus for mux\_2x1\_df\_vhdl

**Library** IEEE;

**use** IEEE.Std\_Logic\_1164.all;

-- Note: select is a reserved word

**entity** t\_mux\_2x1\_df\_vhdl **is**

**end** t\_mux\_2x1\_df\_vhdl;

**architecture** Dataflow **of** t\_mux\_2x1\_df\_vhdl **is**

**signal** t\_A, t\_B, t\_C: Std\_Logic;

**signal** t\_sel: Std\_Logic;

**signal** t\_mux\_out: Std\_Logic;

**component** mux\_2x1\_df\_vhdl

**port** (A, B: **in** Std\_Logic; C: **out** Std\_Logic; sel: **in** Std\_Logic);

**end component**;

**begin**

**process begin**

-- Stimulus signal assignments

    t\_sel <= '1'; t\_A <= '0'; t\_B <= '1'; t\_C <= '0';

**wait for** 10 ns;

    t\_A <= '1';

    t\_B <= '0'; t\_C <= '1';

**wait for** 10 ns;

    t\_sel <= '0';

**wait for** 10 ns;

    t\_A <= '0'; t\_B <= '1'; t\_C <= '1';

**end process**;

-- Instantiate UUT

    M0: mux\_2x1\_df\_vhdl **port map** (a => t\_A, B => t\_B, C => t\_C,

    sel => t\_sel);

**end** Dataflow;