

```
entity full_adder_vhdl is  
    port (S, C: out Std_Logic; x, y, z: in Std_Logic);  
end full_adder_vhdl  
  
architecture Structural of full_adder_vhdl is  
    signal S1, C1, C2: Std_Logic;  
    component half_adder_vhdl (S, C, port x, y, z);  
begin  
    HA1: half_adder_vhdl port map (S => S1, C => C1, x => x, y => y);  
    HA2: half_adder_vhdl port map (S => S, C => C2, x => S1, y => z);  
    C <= C2 or C1;  
end Structural;
```