entity full\_adder\_vhdl is

port (S, C: out Std\_Logic; x, y, z: in Std\_Logic);

end full\_adder\_vhdl

architecture Structural of full\_adder\_vhdl is

signal S1, C1, C2: Std\_Logic;

component half\_adder\_vhdl (S, C, port x, y, z);

begin

HA1: half\_adder\_vhdl port map (S => S1, C => C1, x => x, y => y);

HA2: half\_adder\_vhdl port map (S => S, C => C2, x => S1, y => z);

C <= C2 or C1;

end Structural;