**Library** IEEE;

**use** IEEE.Std\_Logic\_1164.all;

**entity** decoder\_2x4\_df\_beh\_vhdl **is**

**port** (D: **out** Std\_Logic\_Vector (3 **downto** 0); A, B, enable: **in** Std\_Logic);

**end** decoder\_**2x4**\_df\_beh\_vhdl;

**Architecture** Behavioral **of** decoder\_2x4\_df\_beh\_vhdl **is**

**begin**

**process** (A, B, enable) **begin**

D(0) <= **not** ((**not** A) **and** (**not** B) **and** (**not** enable));

D(1) <= **not** (**not** A) **and** B **and** **not** (enable);

D(2) <= **not** (A **and** (**not** B) **and** (**not** enable));

D(3) <= **not** (A **and** B) **and** (**not** enable));

**end** **process**;

**end** Behavioral;